सत्यमेव जयते

INTELLECTUAL PROPERTY **INDIA**

GOVERNMENT OF INDIA
MINISTRY OF COMMERCE & INDUSTRY,
PATENT OFFICE, DELHI BRANCH,
W - 5, WEST PATEL NAGAR,
NEW DELHI - 110 008.

CERTIFIED COPY OF PRIORITY DOCUMENT

I, the undersigned being an officer duly authorized in accordance with the provision of the Patent Act, 197 0 hereby certify that annexed hereto is the true copy of the ***Application, Complete Specification*** *and* ***Drawing Sheets*** *filed in connection with Application for Patent No.**323/Del/03** dated **20th March 2003.***

Witness my hand this 22nd day of March 2004.

(S.K. PANGASA)
Assistant Controller of Patents & Designs

G11C15/00

0323-DEL-03

FORM 1 20 MAR 2003

THE PATENTS ACT, 1970
(39 of 1970)
APPLICATION FOR GRANT OF A PATENT
(See Sections 5(2), 7, 54 and 135)

1. I/we,

STMicroelectronics Pvt. Ltd., an Indian company, of Plot No. 2 & 3, Sector 16A, Institutional Area, Noida – 201 3001, Uttar Pradesh, India.

2. hereby declare –

(a) that I am/we are in possession of an invention titled ***"A Content Addressable Memory (CAM) Architecture Providing Improved Speed."***

(b) that the ~~provisional~~ / complete specification relating to this invention is filed with this application

(c) that there is no lawful ground of objection to the grant of a patent to me/us.

3. further declare that the inventor(s) for the said inventions is/are

(i) SRIVASTAVAAN Rajeev, an Indian national, of 16/301, East End Apartments, Mayur Vihar Phase – I Extn., Delhi – 110 096, India.

(ii) GROVER Chiranjeev, an Indian national, of 1501/D/34, Mohan Park, Naveen Shahdara, Delhi – 110 032, India.

ORIGINAL

5. I/we claim the priority from the application(s) filed in convection countries, particulars of which are as follows: **NA**

5. I/we state that the said invention is an improvement in or modification of the invention the particulars of which are as follows and of which I/we are the applicant/patentee: **NIL**

6. I/we state that the application is divided out of my/our application, the particulars of which are given below and pray that this application be deemed to have been filed on under section 16 of the Act. **NIL**

7. That I am/we are the assignee or legal representative of the true and first inventors.

8. That my/our address for service in India is as follows:

ANAND & ANAND, Advocates
B-41, Nizamuddin East
New Delhi – 110 013

Tel Nos.: (11) 24355078, 24355076, 24350360

9- I/We the true and first inventors of this invention or the applicant(s) in the convention country declare that the applicant(s) herein is/are my/our assignee or legal representative.

a) *Rajeev Srivastavaan Indian National of 16/301, East End Apartments, Mayur Vihar Phase-I Extn., Delhi 110096*

Signature

Rajeev Srivastava

Dated this 20th day of March 2003

b) Chiranjeev Grover an Indian National of 1501/D/34, Mohan Park, Naveen Shahdara, Delhi 110032

Signature

Chiranjeev Grover

Dated this 20th day of March 2003

10- that to the best of my/our knowledge, information and belief the fact and matters stated herein are correct and that there is no lawful ground of objection to grant of patent to me/us on this application.

11- Following are the attachment with the application

(a) Complete specification (3 copies)
(b) Abstract
(c) Formal drawings
(d) Power of Attorney
(e) Form 1 (in triplicate)
(f) Form 3 (in duplicate)
(g) Fee Rs. 5000/- In cash/cheque/bank draft bearing no. , date On Bank.

I/We request that a patent may be granted to me/us for the said invention.

Dated this 20th day of March 2003

Signature
STMicroelectronics Pvt. Limited

To

The Controller of Patents
The Patent Office, Delhi

02-IND-369

0323-03

Form 2

THE PATENTS ACT, 1970

20 MAR 2003

COMPLETE SPECIFICATION

[See Section 10]

A CONTENT ADDRESSABLE MEMORY (CAM) ARCHITECTURE PROVIDING IMPROVED SPEED

ORIGINAL

***STMicroelectronics Pvt. Ltd.**, Plot No. 2 & 3, Sector 16A, Institutional Area, Noida – 201 301, Uttar Pradesh, India, an Indian Company*

The following specification particularly describes and ascertains the nature of this invention and the manner in which it is to be performed

A CONTENT ADDRESSABLE MEMORY (CAM) ARCHITECTURE PROVIDING IMPROVED SPEED

Field of the Invention

The invention relates to the field of binary Content Addressable Memory (CAM) applications. More particularly the invention relates to a method and device providing improved performance by utilizing both phases of the clock cycles.

Background of the Invention

A content addressable memory CAM architecture is an array of individual CAM cells. Each CAM cell consists of a data storage unit and comparison circuitry. The storage unit is used for storing data and the comparison circuitry is used to compare the compare-data with the data stored in storage unit and providing a signal indicating a match or mismatch. This signal is fed to a priority encoder for selecting one of the match signal, in the vent of multiple as the final output.

Throughout this disclosure, logical "1" refers to and is interchangeable with a logical "**High**" corresponding to a voltage **VDD**, while logical "0" refers to and is interchangeable with a logical "**Low**" corresponding to **GND**. **Figure1** illustrates a prior art 9-transistor CAM cell **100** using a NOR configuration. The CAM cell **100** includes an SRAM cell for data storage, comprising a pair of cross-coupled inverters formed by transistors **111**, **112**, **113** and **114** and a pair of access transistors **115** and **116**. The comparison circuitry of the CAM cell **100** consists of a pair of pass transistors **117** and **118**. The conducting terminals of the pass transistor **113** and **111** are connected in series between the supply voltage **VDD** and ground **GND** while the control terminals are connected to the common conducting terminals **F** of pass transistors **114** and **112**. The conducting terminals of pass transistor **114** and **112** are also connected in series between **VDD** and **GND** while the control terminals are connected to the common conducting terminals **T** of pass transistors **113** and **111**. The conducting terminals of pass transistors **115** and **116** connect nodes **T** and **F** to the corresponding bit lines **BLT** and **BLF** while the control terminals are connected to word line **WL**. The pass transistors **117** and **118** are connected in series between bit lines **BLT** and **BLF** and the common node is labeled as the **Bit-Match** node. The control terminals of transistors **117** and **118** are coupled to nodes **F** and **T**, respectively. Output transistor **119** is coupled between the match line **ML** and ground **GND** and its control terminal is connected to the **Bit-Match** node of the CAM cell.

The READ and WRITE operations of this CAM cell **100** are the same as those of a standard 6-transistor SRAM cell, wherein the precharge state of bit lines **BLT** and **BLF** is logical "High". During the SEARCH operation, bit lines **BLT** and **BLF** are initially precharged to logical "Low" and **ML** is precharged to logical "High". Then the comparand bit is placed on **BLT** and its complement is placed on **BLF**. If the comparand bit matches with the data bit stored in the CAM cell, then one of the pass transistors **117** or **118** drives the **Bit-Match** node to logical "0" and therefore ML remains at logical "High", indicating a match. On the other hand, if there is a mismatch between the applied comparand bit and the data bit stored in the CAM cell, then one of the pass transistors **117** or **118** drives the Bit-Match node to "VDD-Vtn", thereby turning the pull-down transistor **119** on and pulling down **ML** indicating a mismatch.

The CAM cell **100** requires a precharge to logical "Low" operation for bit lines and a precharge to logical "High" operation for **ML** when a SEARCH operation is requested if the default standby state is for a READ or a WRITE operation. Conversely, if the CAM cell **100** is ready for a SEARCH operation in its default standby state, then the bit lines must be precharged to logical "High" and **ML** is thereby discharged when a READ or WRITE operation is requested. It is known that both bit lines and **ML** impose a heavy capacitive load on their drivers and prechargers. Therefore, CAM cell **100** consumes more power and provides larger READ/WRITE/ SEARCH access times.

Figure 2 illustrates another prior art 9-transistor CAM cell **200** using a NOR configuration. The only difference between CAM cell **100** and **200** is that CAM cell **200** is provided with dedicated lines **CBLT** and **CBLF** for the search operation as shown in the **figure 2**. Thus, CAM cell **200** provides more flexibility in the timing of READ, WRITE and SEARCH operations but at the cost of hardware overhead required for controlling the dedicated compare bit lines **CBLT** and **CBLF.**

Object and Summary of the Invention

The object of the invention is to obviate the above drawbacks and provide memory architecture with higher speed and smaller size.

Another object of the invention is to combine compare and write or compare and read operation in one clock cycle to increase the speed of operation without increasing the area of the chip.

To achieve the said objectives, this invention provides a Content Addressable Memory (CAM) architecture providing improved speed, comprising:

- an array of CAM cells connected to a compare-data-write-driver and to a read/write block, for receiving the compare-data and for reading and/or writing data in the array of CAM cells respectively,
- outputs of the said CAM cell are coupled to a match block providing match outputs signal lines that identifies a match/no-match at the end of a search operation, and;
- a control logic for implementing search and address decoding operations during first state and enabling read-or-write operations within the second state of the same clock cycle in the event of a match.

The control logic comprising a sequencing circuit that enables the data comparators of the CAM cell array and the address decoder of read/write block during the first state of the clock and enables the read-or-write operation in the second state of the same clock.

The invention further provides a method for improving speed of a Content Addressable Memory (CAM) architecture in steps of:

- connecting an array of CAM cells to a compare-data-write-driver and to a read/write block, for receiving the compare-data and for reading and writing data in the CAM cell respectively,
- coupling a match block to said array of CAM cell providing match outputs signal lines for identifying a match/no-match at the end of a Search operation,
- performing the search and address decoding operations during first state of the clock cycle, and;
- implementing the read/write operation after a successful search during the second state of the same clock cycle.

Brief Description of the Drawings:

The invention will now be described with reference to the accompanying drawings.

Figure 1 shows a conventional 9-transistor CAM cell architecture.

Figure 2 shows another conventional 9-transistor CAM cell architecture.

Figure 3 shows a block diagram of a CAM architecture in accordance with the present invention.

Figure 4 shows a data flow chart of a decoder.

Figure 5 shows a data flow chart for the normal read and write operation.

Figure 6 shows a timing diagram for the normal read operation.

Figure 7 shows a timing diagram for the normal write operation.

Figure 8 shows a timing diagram for the normal compare operation.

Figure 9 shows a timing diagram for the combine operation of compare and read.

Figure 10 shows a timing diagram for the combine operation of compare and write.

Detailed Description of the Drawings

Figures 1 and **2** have already been described under the background to the invention.

Figure 3 shows a block diagram of a CAM memory architecture in accordance with the present invention. The instant invention uses a **Control Block** for performing read/write and compare operations in parallel. The **Control Block** provides the flexibility to choose either to perform any one of the read/write/compare operations in normal mode or to perform the read/write and compare operations in combined mode.

In the normal mode compare operation the **Control Block** uses the **Compare Data Write Driver** to feed the compare data into the memory core through the bit lines. The bitline data is compared with the data stored in each cell of the Core. The results of the compare operation are then fed to the **Match Block.** The **Match block** generates a hit signal for the highest priority matching data. The **Match block** also provides a match/mismatch signal to the ROM encoder/Cache.

The **Control Block** sends a signal to **Read/Write Block** during the normal mode read/write operation. The address of the memory cell is decoded by the decoder with in the **Read/Write Block**. In case of a read operation, the word line corresponding to decoded address is enabled

to provide the data contained in the memory at the bit lines. The data at the bit lines is then sensed by a sense amplifier. The output of the sense amplifier is latched in the output latch. In the case of a write operation, decoding is performed in a similar manner. Once the word line is selected, the data present at the Data input register is written on the selected line through a **Write Driver**.

For the combined compare and write operation, the address decoding and comparing are performed in the first half of the clock cycle. In the second half of the clock cycle the world line corresponding to the decoded address is enabled and the **Write driver** then performs the write operation.

For the combined compare and read operation, the address decoding and comparing are performed in first half of the clock cycle. In the second half of the clock cycle the world line corresponding to the decoded address is enabled, to provide the data contained in the memory at the bit lines. The data at the bit lines is then sensed by a sense amplifier. The output of sense amplifier is latched in the output latch.

Figure 4 shows a data flow diagram of the decoder used for decoding the memory addresses. The decoder block has the input **Address Registers** followed by **Address Buffers**. The address is decoded in two stages with two **Pre-Decoder Blocks**. The **Final Decoder** stage generates the complete word line address.

Figure 5 shows a data flow diagram for the normal read and write operation. For write operation the data is loaded into the **Data I/P Register.** The **Write Driver** receives the data input from the **Data I/P Register** and assigns the data to the respective bit lines of the **CAM Core**. A latch based sense amplifier and a data output latch are provided for a Read operation. The output latch preserves the last read data until the next read cycle. When there is no read/write operation, the bit lines are precharged to "high".

Figure 6 shows the timing diagram of a normal read operation. =As shown in the figure **Comp_En** is disabled on the positive edge of the clock cycle, , and read enable line **Read_En** is enabled. The decoder provides the **Address** of the memory to be read, and when the complete address is available the **Word Line** corresponding to the decoded address is

enabled thereby providing data content in the memory cell to the bit lines. The data is sensed by a sense amplifier and made available at the **Data Out**.

Figure 7 shows the timing diagram of a normal write operation. As shown in the figure, **Comp_En** is disabled at the positive edge of the clock cycle, and write enable line **Write_En** is enabled. The decoder provides the **Address** of the memory to be written, and when the complete address is available, the bit lines corresponding to the address are provided with the data, while the associated **Word Line** is enabled connecting the bit lines to the memory cell.

Figure 8 shows the timing diagram for a normal compare operation. As shown in the figur **Comp_En** is enabled at the positive edge of the clock cycle, and, the compare data signal **Comp_Data** is enabled providing the data at the **bit lines**. Depending upon Match/mis-Match a **hit/miss** is generated.

Figure 9 shows the timing diagram for a combined compare and read operation.. In the positive phase of the clock cycle, the compare and decoding operation are performed generating a hit/miss signal. The hit/miss signal is latched for each row of the core at the falling edge of the clock. The address decoder is also activated at the positive edge of the clock for selecting a word line for the read operation from the memory. The Address is decoded for the output of the Predecoder stage or the input of the final decoder stage. The negative clock cycle triggers the reading action enables the final decoder and selects the wordline corresponding to the address for the read operation.

Figure 10 shows the timing diagram for the combined compare and write operation. The compare and decoding operations are performed at the positive phase of clock generating a hit/miss signal. The hit/miss signal is latched for each row of the core at the falling edge of the clock. The positive phase of clock also activates the address decoder for selecting a word line for the write operation from the memory. The Address is decoded upto the output of the Predecoder stage or the input of the final decoder stage. The negative edge of the clock cycle triggers the writing action enables the final decoder and selects the wordline corresponding to the address input for the write operation.

It will be apparent to those with ordinary skill in the art that the foregoing is merely illustrative intended to be exhaustive or limiting, having been presented by way of example only and that various modifications can be made within the scope of the above invention.

Accordingly, this invention is not to be considered limited to the specific examples chosen for purposes of disclosure, but rather to cover all changes and modifications, which do not constitute departures from the permissible scope of the present invention. The invention is therefore not limited by the description contained herein or by the drawings, but only by the claims.

We Claim:

1. A Content Addressable Memory (CAM) architecture providing improved speed, comprising:
   - an array of CAM cells connected to a compare-data-write-driver and to a read/write block, for receiving the compare-data and for reading and/or writing data in the array of CAM cells respectively,
   - outputs of the said CAM cell are coupled to a match block providing match outputs signal lines that identifies a match/no-match at the end of a search operation, and;
   - a control logic for implementing search and address decoding operations during first state and enabling read-or-write operations within the second state of the same clock cycle in the event of a match.

2. A CAM architecture as claimed in claim 1, wherein the control logic comprising a sequencing circuit that enables the data comparators of the CAM cell array and the address decoder of read/write block during the first state of the clock and enables the read-or-write operation in the second state of the same clock.

3. A method for improving speed of a Content Addressable Memory (CAM) architecture in steps of:
   - connecting an array of CAM cells to a compare-data-write-driver and to a read/write block, for receiving the compare-data and for reading and writing data in the CAM cell respectively,
   - coupling a match block to said array of CAM cell providing match outputs signal lines for identifying a match/no-match at the end of a Search operation,
   - performing the search and address decoding operations during first state of the clock cycle, and;
   - implementing the read/write operation after a successful search during the second state of the same clock cycle.

4. A Content Addressable Memory (CAM) architecture providing improved speed substantially as herein described with reference to and as illustrated in the accompanying drawings.

5. A method for improving the speed of operation of a Content Addressable Memory (CAM) cell substantially as herein described with reference to and as illustrated in the accompanying drawings.

Dated this 26th day of March 2003

of **ANAND & ANAND, Advocates**
Agents for the Applicants

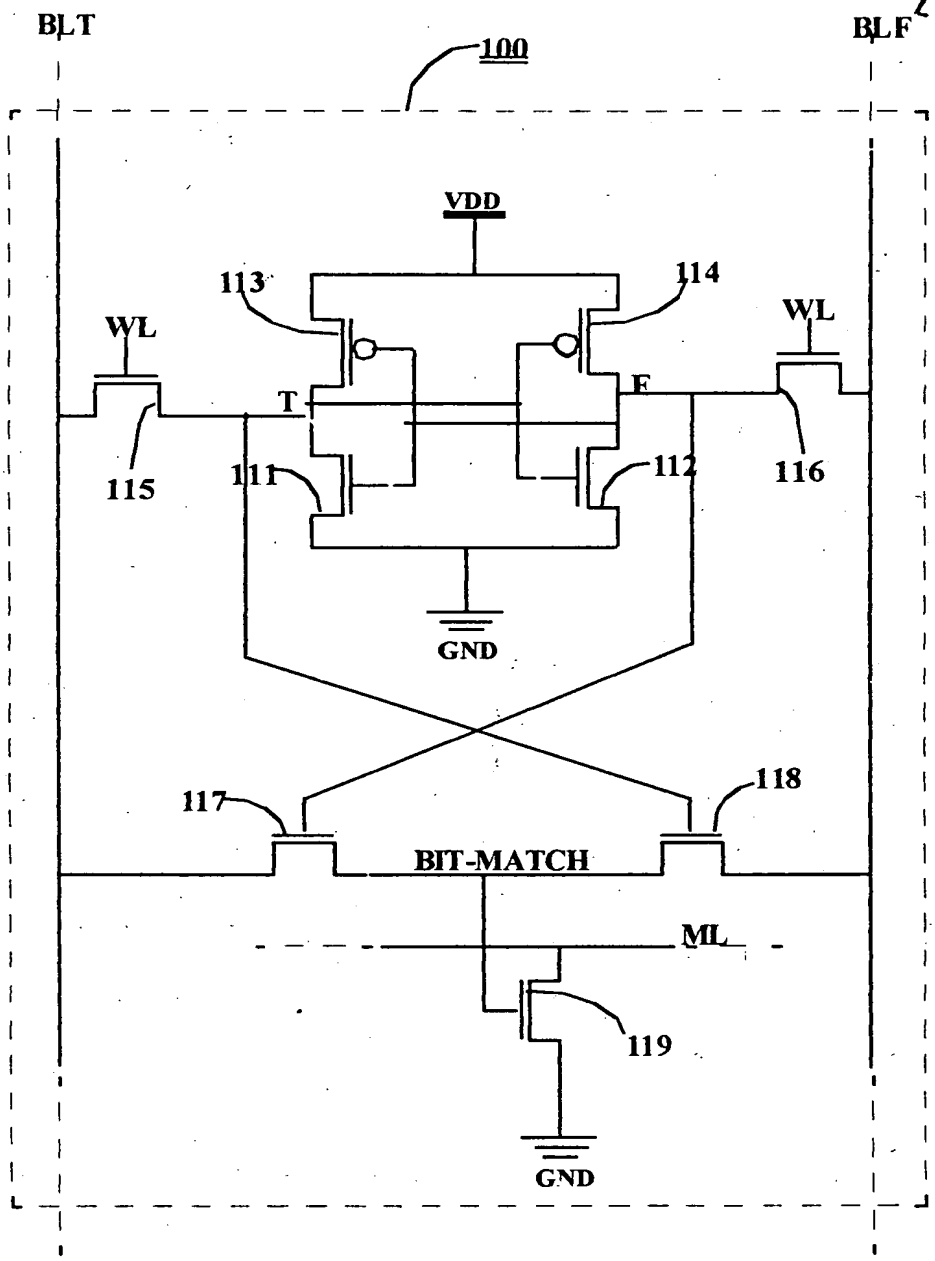

FIG. 1 : PRIOR ART

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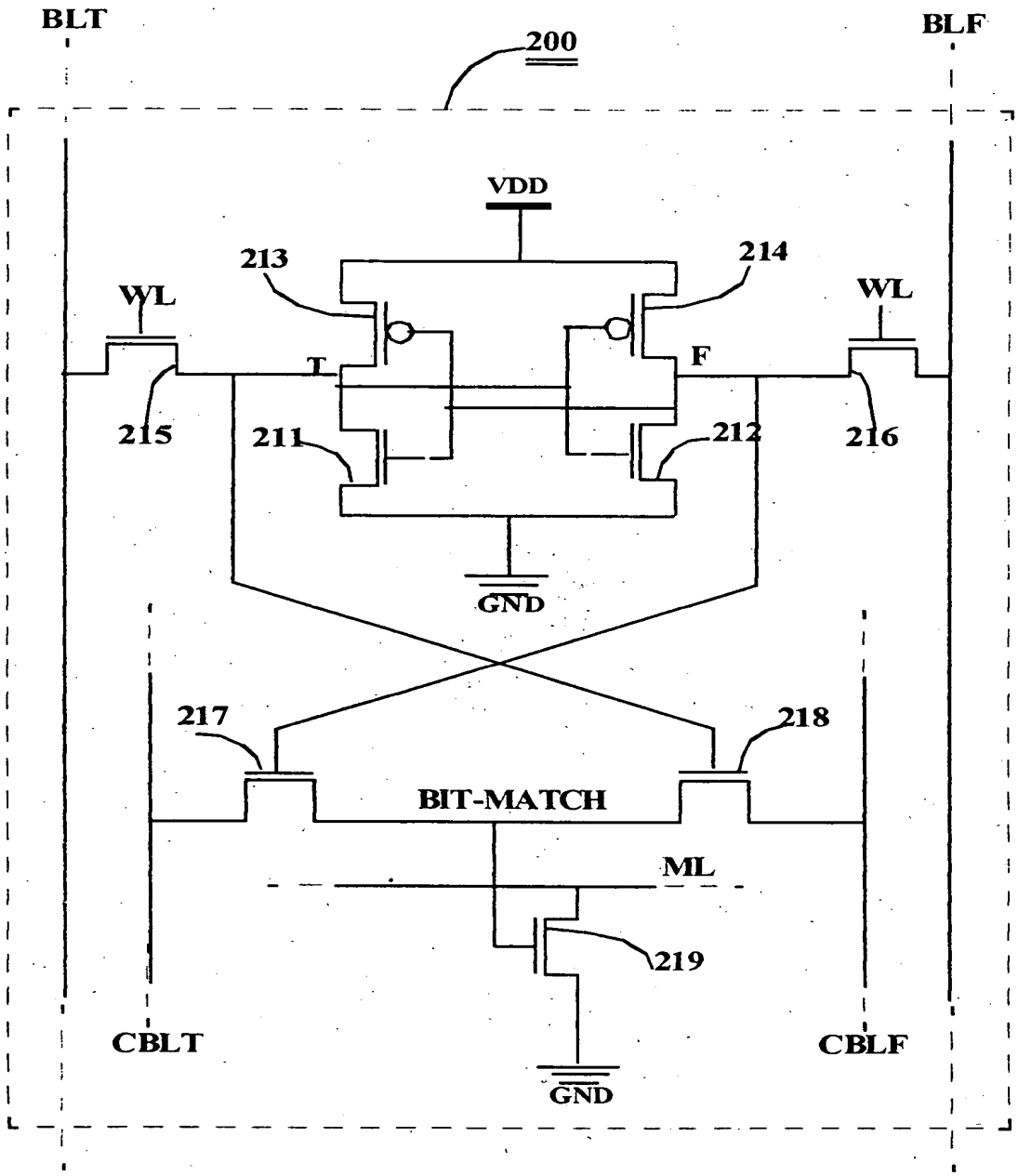

FIG. 2 : PRIOR ART

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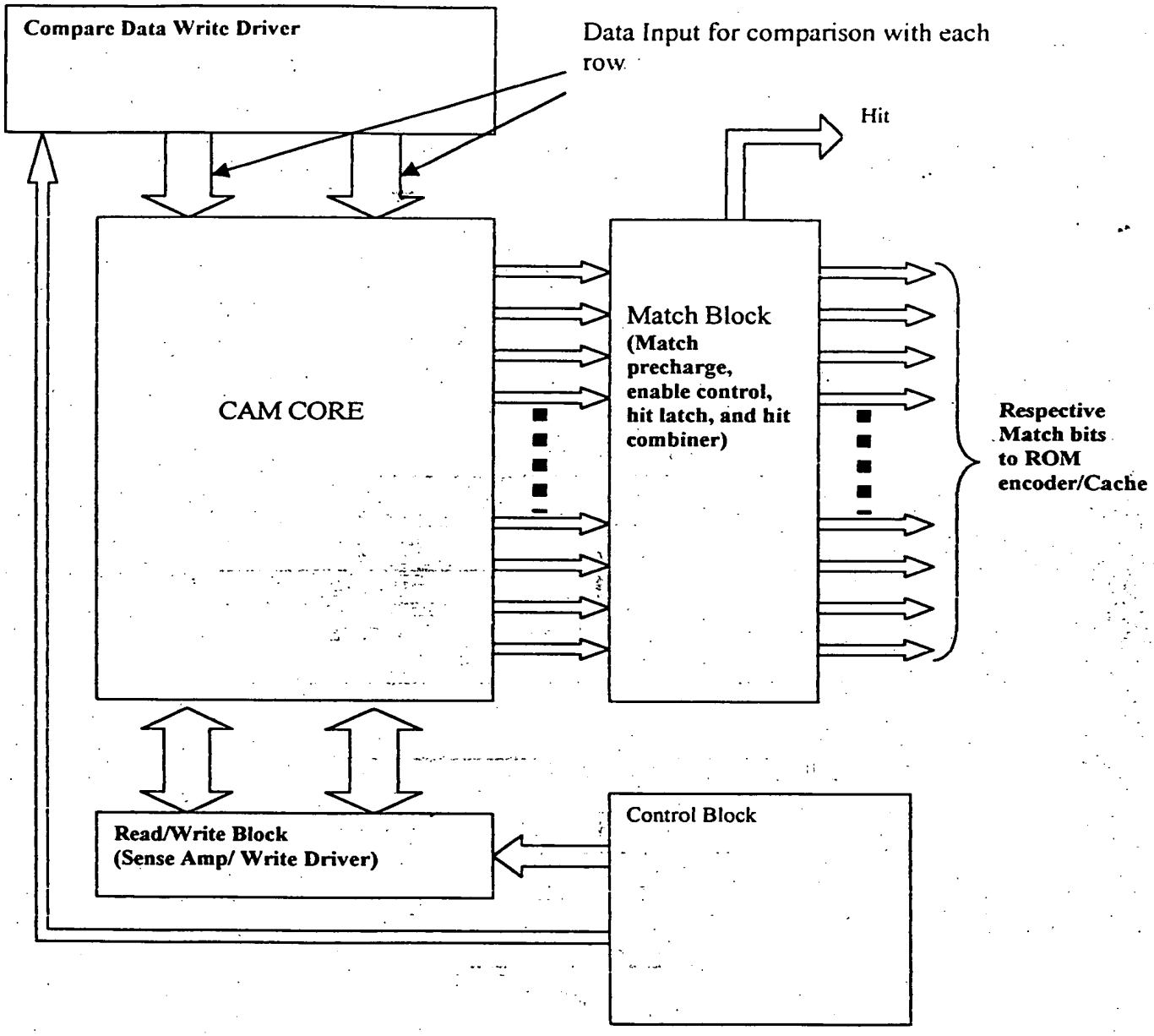

Figure No.3 : The full Architecture

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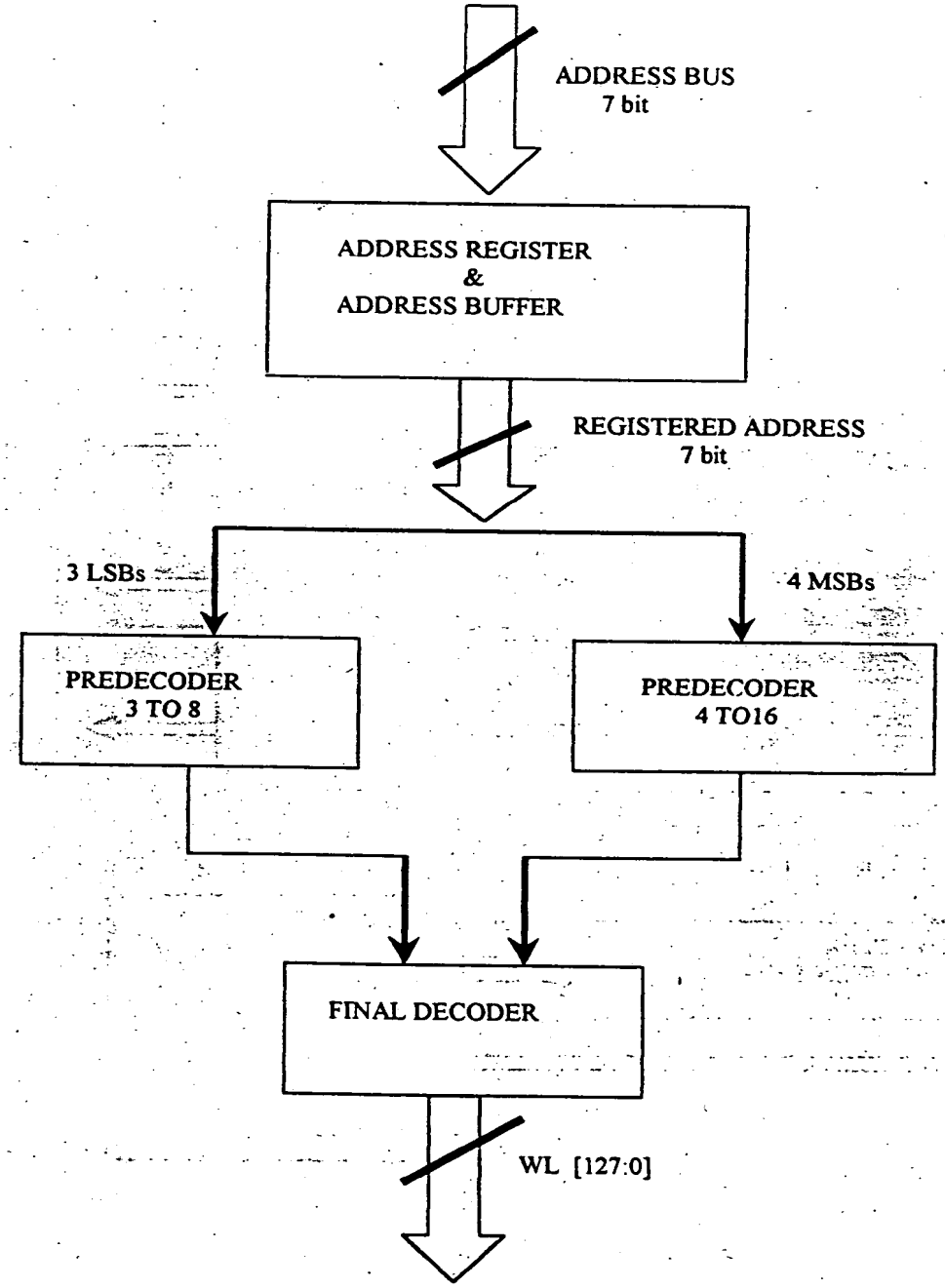

Figure 4: Decoder Block

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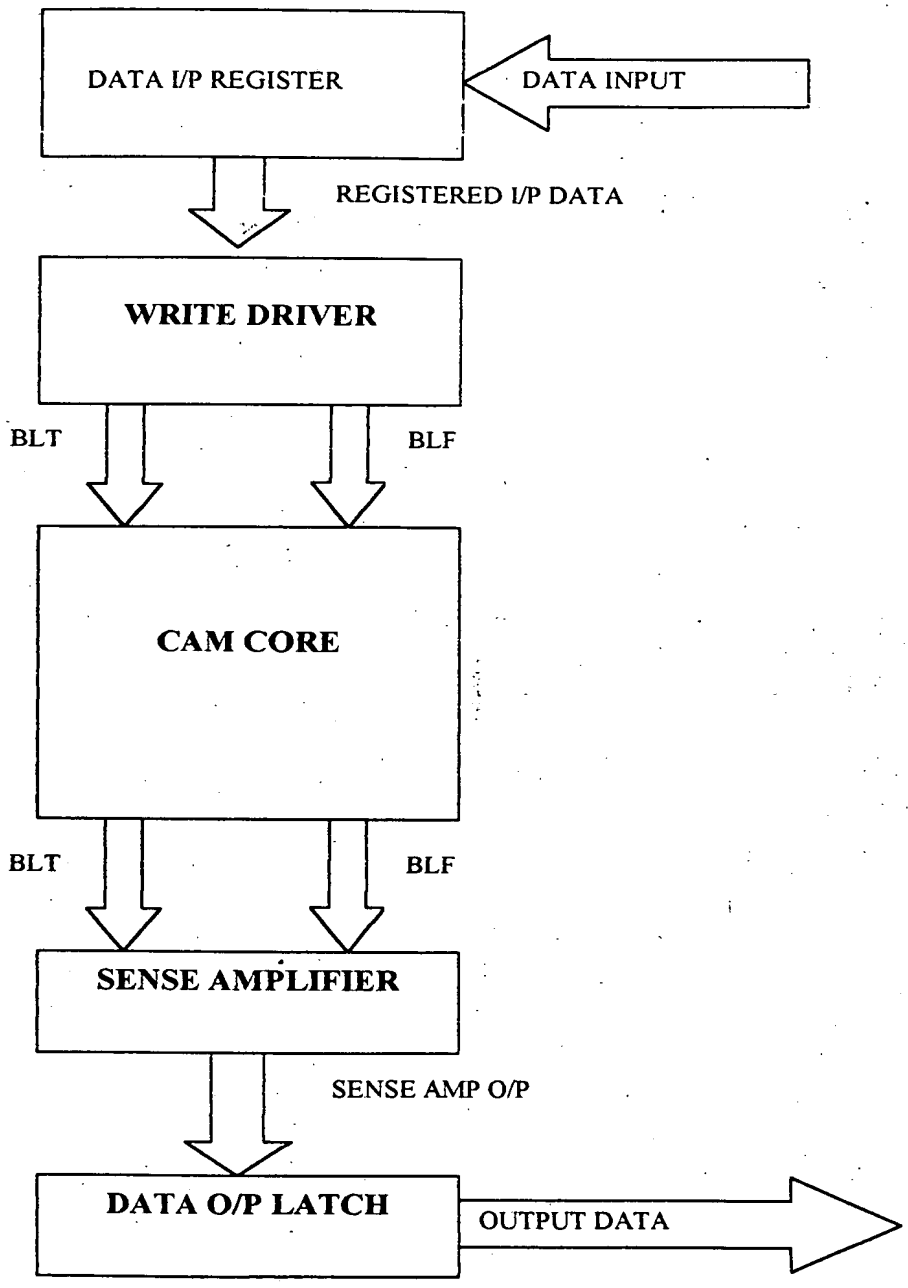

Figure No. 5 : Normal Read Write Operation in CAM

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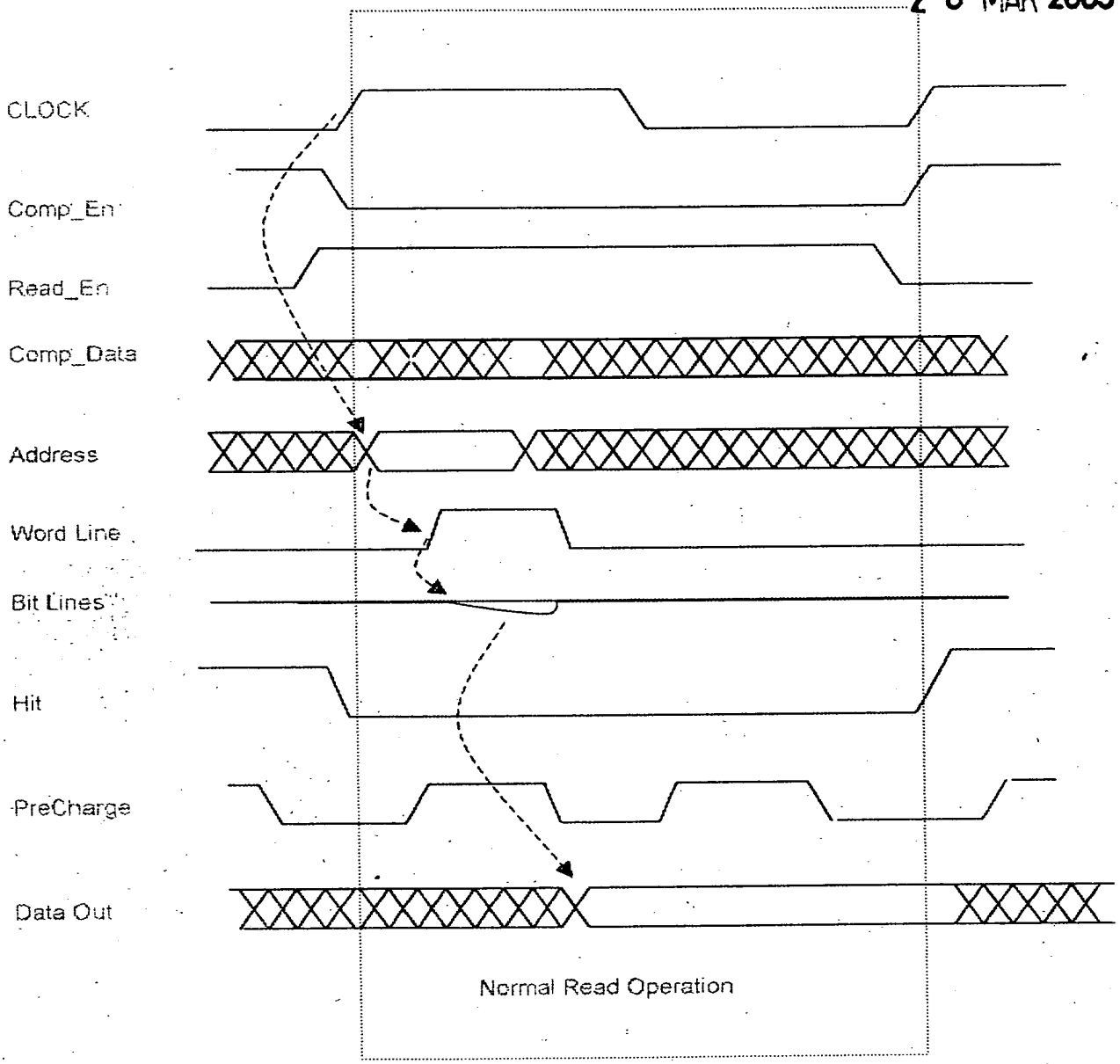

DUPLICATE

Figure 6 : Wave Form for Normal Read Operation

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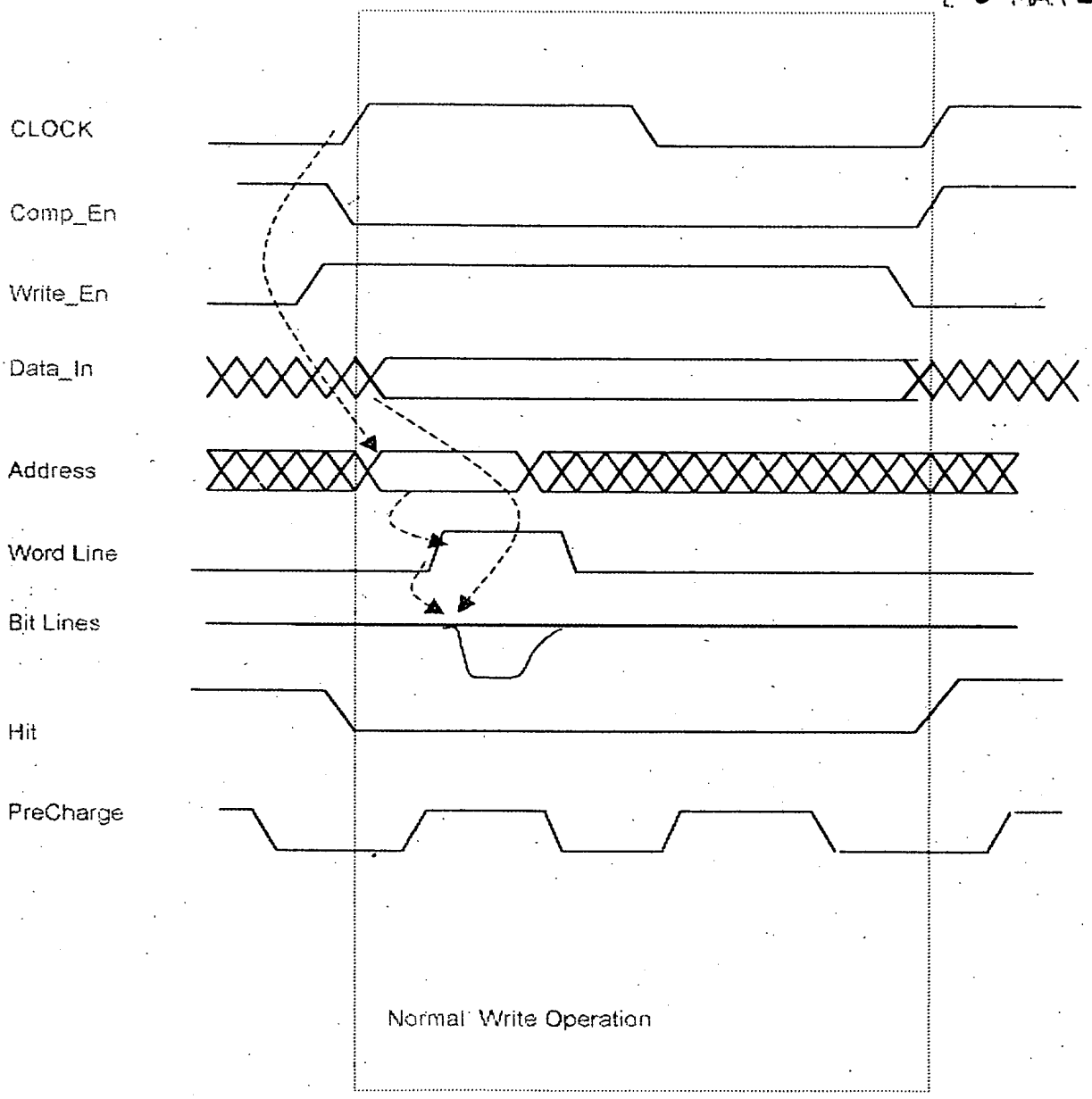

Figure7 Normal Write Operation

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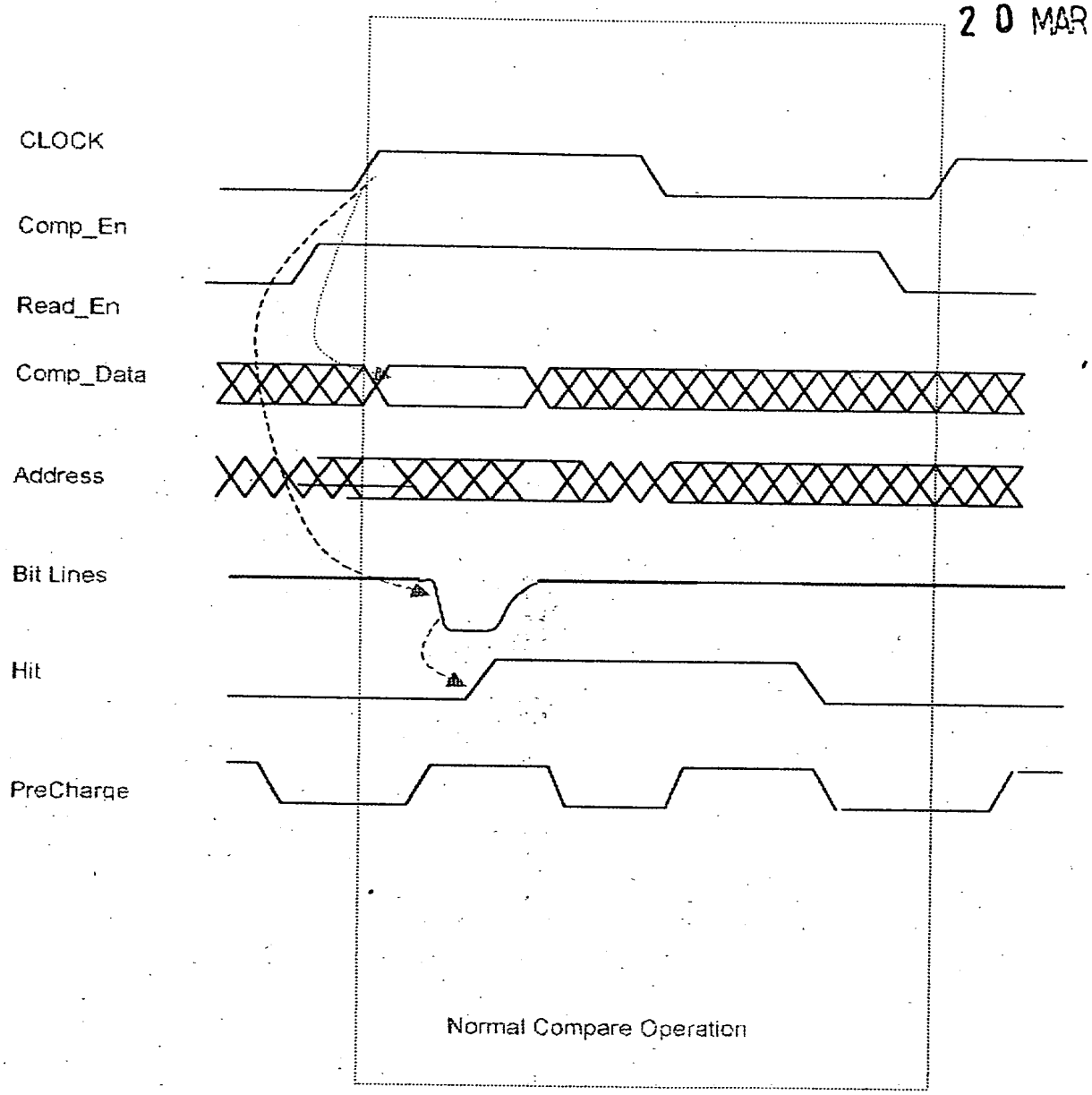

Figure 8 Normal Compare Operation

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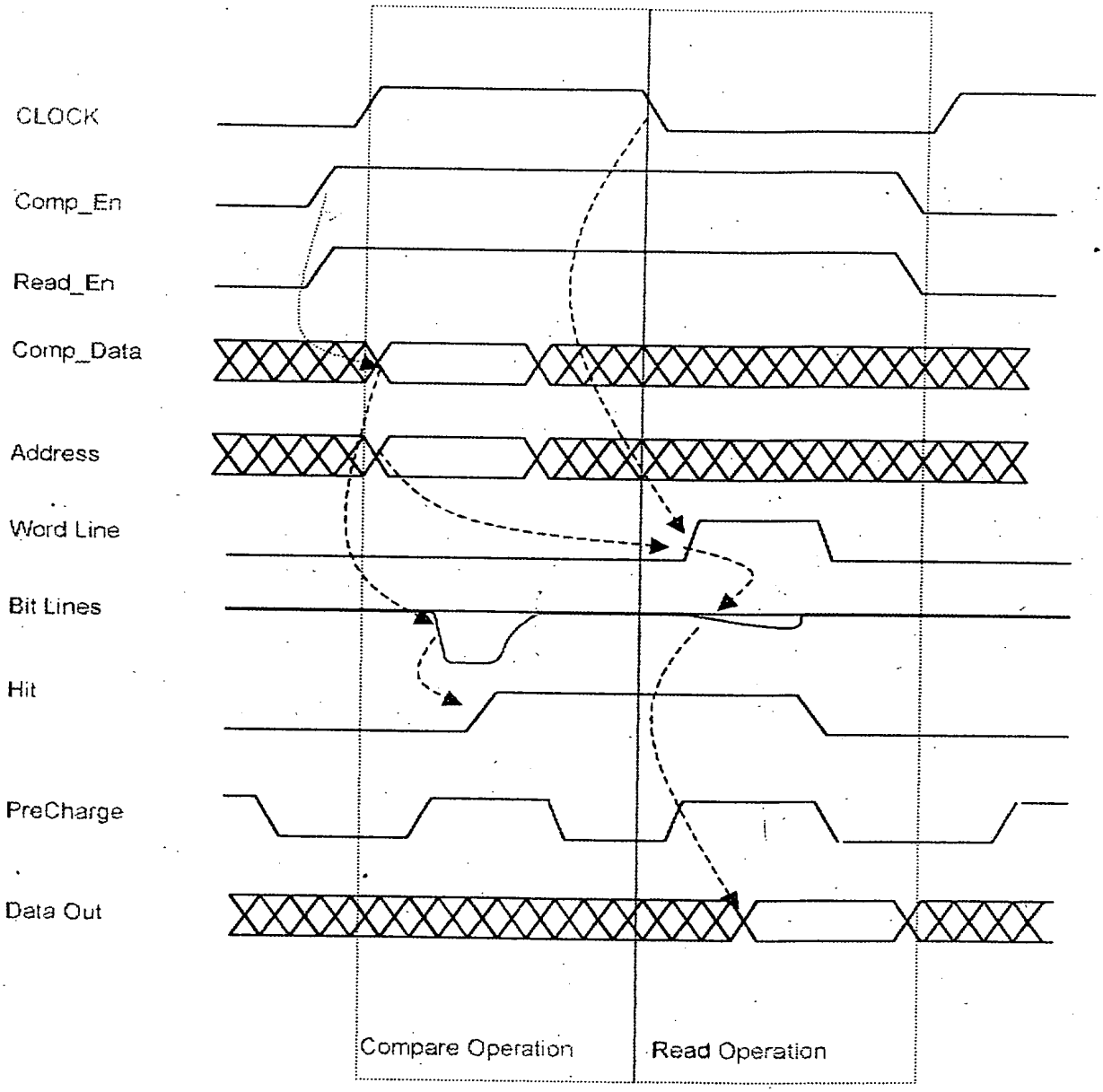

Figure 9 Compare & Read Operation in one Cycle

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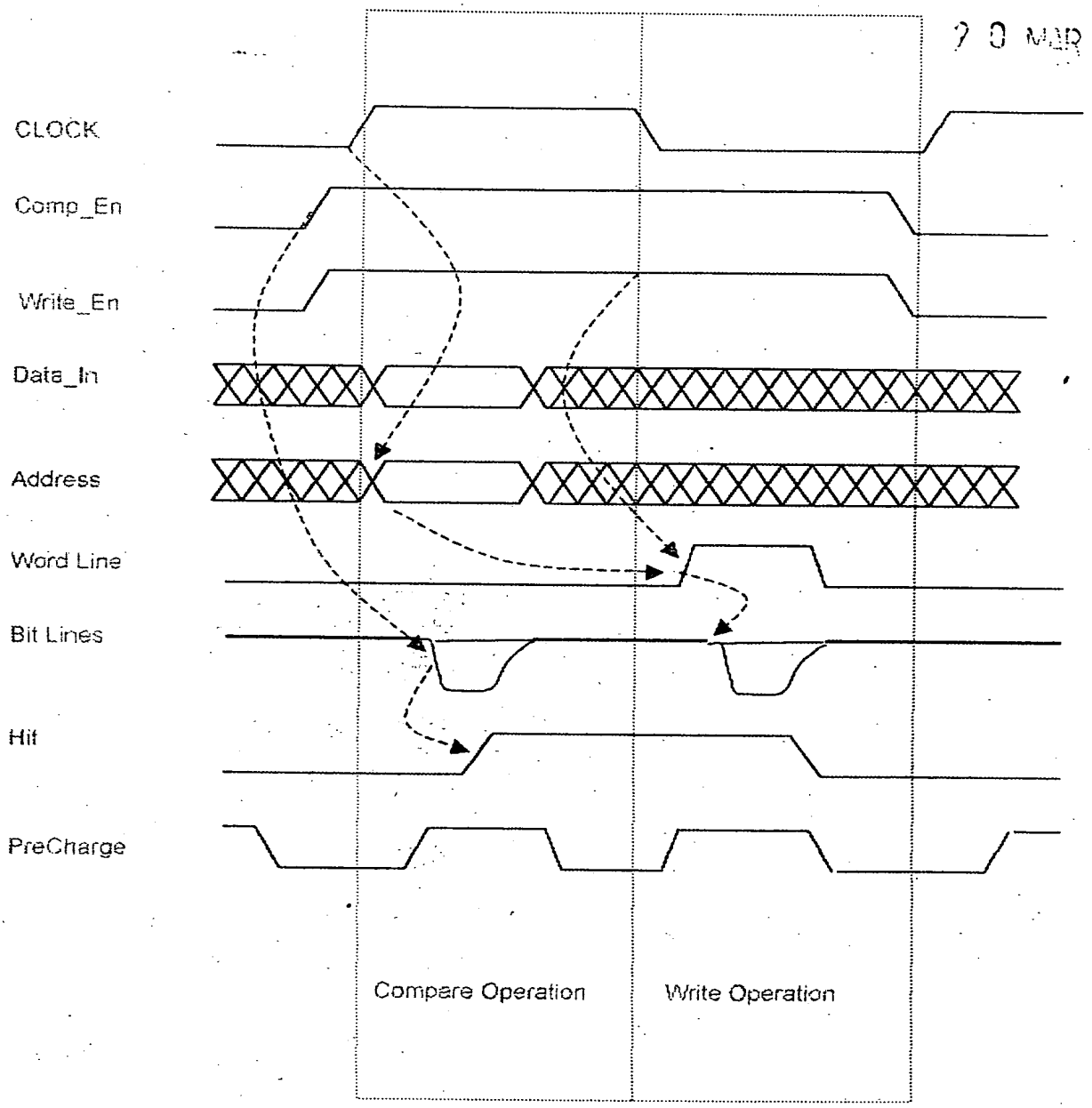

Figure 10 Compare & Write Operation in one Cycle

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Agents for the Applicants

ABSTRACT

This invention provides a Content Addressable Memory (CAM) architecture providing improved speed by performing mutually exclusive operations in first state of a clock cycle and by performing at least one operation, dependent on at least one previous operations, in the second state of the same clock cycles. The Content Addressable Memory (CAM) architecture comprises an array of CAM cells connected to a compare-data-write-driver and to a read/write block, for receiving the compare-data and for reading and/or writing data in the array of CAM cells respectively, outputs of the said CAM cell are coupled to a match block providing match outputs signal lines that identifies a match/no-match at the end of a search operation, and a control logic for implementing search and address decoding operations during first state and enabling read-or-write operations within the second state of the same clock cycle in the event of a match.